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501.43211X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: S. MISAKA, et al

Serial No.: 10/694,849

Filed: October 29, 2003

For: POWER CONSUMPTION REDUCTION AND QUICKER
INTERRUPTION RESPONSE IN AN INFORMATION
PROCESSING DEVICE UTILIZING A FIRST TIMER AND A
SECOND TIMER WHEREIN THE SECOND TIMER IS ONLY
CONDITIONALLY ACTIVATED (Amended)

Group: 2115

Examiner: S. Suryawanshi

INFORMATION DISCLOSURE STATEMENT (IDS)

MS Amendment

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

August 21, 2007

Sir:

Applicants are enclosing herewith copies of JP 07-152588; JP 62-009418 and JP 01-187619 for placement in the file of the present application.

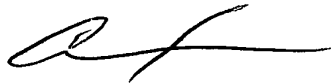
This document came to Applicants attention in an Office Action received from a foreign patent office during the examination of a corresponding application.

The cited documents are not believed to raise a prima facie case of unpatentability with respect to any of the allowed claims, whether taken individually or in combination with any of the other prior art of record.

Although the Examiner is not required to consider these documents at this stage of prosecution, Applicants wish their placement in the file for the benefit of the public.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C. Deposit Account No. 50-1417 (501.43211X00) please credit any excess fees to such deposit account.

Respectfully submitted,



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MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.



1. IDS based on the Office Action for Japanese counterpart

In the office action, the Japanese examiner referred to the following three references. All references #1-#3 have no English counterpart publications. So we are informing you of the Japanese examiner's comments and the English abstracts in the office action. Please file the Japanese examiner's comments and the English abstracts as concise explanations.

#	Japanese Publication No. referred in the office action	English counterpart publications No.
1	JP07-152588	-
2	JP62-009418	-
3	JP01-187619	-

Japanese Examiner's Comments in the Office Action.

In reference 1, paragraphs (0013) to (0027) describes the following: "A task wait time management unit includes a system timer 6 (corresponding to a first timer circuit in this application) and a real timer 7 (corresponding to a second timer circuit in this application), and when a task execution request specifying a wait time T_s is made, a fraction time T_r is read from the real timer, time $(T_s - T_r)$ obtained by subtracting that fraction time T_r from the wait time T_s is divided by a normal period T_o to calculate a quotient N and a remainder time n , and that quotient N is specified as a stick number in a system timer queue. According to the occurrence of a periodic interrupt request after a numeric normal period $(N \cdot T_o)$ corresponding to the stick number N , setting the remainder time n in a real timer wait queue starts the corresponding task after the remainder time n elapses."

Paragraphs (0015) and (0047) describes that the system timer 6 makes an interrupt into a CPU 2 whenever a predetermined normal period T_o such as 100 ms (corresponds to "a first period" in this application) elapses, the real timer 7 counts fine units of time such as 1 ms intervals (corresponds to "a second period" in this application) and makes an interrupt into the CPU 2 when there comes each time t_1 specified in a first area 8a of the real timer queue 8 shown in Fig. 2(b) from the started time.

As reference 2 (lines 7 to 11 in right down column, page 1) describes "timer control LSI capable of setting a timer value from the outside," the capability of inputting a period time can easily be made by a person skilled in the art.

Reference 3 (lines 10 to 14 in right down column, page 2) describes that other major timer (e.g., 4 seconds) is made from a basic timer (e.g., 100 milliseconds) (corresponds to "first and second timers operates according to the same clock and a first period is an integral multiple of a second period" in this application).

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SHEET 1 OF 1

FORM PTO-1449 U.S. Department of
Commerce Patent and Trademark Office**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use several sheets if necessary)

ATTY. DOCKET NO.

501.43211X00

SERIAL NO.

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APPLICANT

S. MISAKA, et al

FILING DATE

October 29, 2003

GROUP

2115**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DA IF APPROP

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER							DATE	COUNTRY	CLASS	SUBCLASS	ABSTRACT
												YES
	7	1	5	2	5	8	8	6/95	Japan			XX
	6	2	9	4	1	8		1/87	Japan			XX
	1	1	8	7	6	1	9	7/89	Japan			XX

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation is considered, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

(Form PTO-1449 [6-4])